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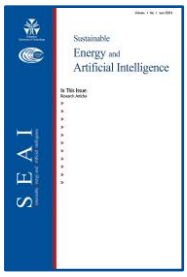

Active Impedance Source Based Inverter with Continuous Source Current

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Abstract

This paper proposes a new active impedance source inverter topology. The proposed inverter provides a continuous source current, appropriate boost-factor, a few numbers of components, low voltage stress on active switch and diodes, low voltage stress across capacitors, and low volume and size. All operating modes of the proposed inverter are analyzed in details, and the design considerations of active and passive components are done. Also, a control method to generate the desired output waveform is proposed. In the following, the comprehensive comparison between the proposed topology and some conventional topologies from different points of view, such as the boost-factor, total voltages across capacitors, total blocked voltages across impedance side diodes, active switch, and volume of passive components are calculated. Ultimately, the simulation results are obtained from a prototype in the PSCAD software. The obtained results from simulation part validate the correctness of operation and performance of the proposed topology as well the given in theoretical part.

Keywords: Impedance Source Inverter; Z-Source Inverter; Active Impedance Source Inverter; Pulse Width Modulation.

1. Introduction

While voltage-source inverters (VSIs) are widely used in various industrial applications, their traditional topologies have certain limitations. For instance, these VSIs can only perform voltage step-down operations and require dead time in their control methods. To achieve a buck/boost operation, an additional DC/DC converter is necessary, which not only reduces efficiency but also increases the system's volume, size, and cost [1,2]. This need for additional components underscores the inefficiency and increased cost of traditional VSIs.

To address the issues mentioned, an impedance-source inverter known as the Z-source inverter (ZSI) was introduced in [3]. The impedance cell consists of two capacitors and two inductors, enabling the topology to function as a buck/boost inverter. This feature allows the ZSI to overcome the typical limitations of short-circuit in voltage-source inverters (VSIs) and ensures its reliability. However, despite the advantages of the ZSI, this topology comes with inherent disadvantages, such as discontinuous input current, lower boost-factor, high voltage across capacitors, and high current through inductors, leading to increased size and cost. To address these problems, another topology called the quasi Z-source inverter (QZSI) was presented in [4]. The QZSI reduces the voltage on the capacitors and decreases the current through the inductors, addressing some of the problems of the ZSI, including size and volume. However, both topologies share the same boost-factor and have a

discontinuous input current. They also consist of an equal number of elements. Various topologies have been proposed in the literature to increase the boost-factor.

The structure of the ZSI and the total time of the shoot-through (ST) state influence the boost-factor of the inverter. Thus, to achieve a higher boost-factor, some studies have focused on control methods [5-7], and others have suggested working on ZSI circuit topologies such as switched-inductor or adding extra passive components [8-12], transformer or coupled-inductor topologies [13-17] and active-switched topologies [18-31]. There are different control methods such as pulse width modulation techniques (PWM) [5-6], Artificial Intelligence (AI) [7]. Applying the switched inductor or adding extra passive components in ZSI can extend the boost-factor. but, in this method, the number of elements is increased. The number of passive elements increases size, cost, volume, and losses [8-12]. A high boost-factor can be achieved without additional components in the transformer or coupled-inductor configurations. The boost-factor is adjustable by modifying the turn ratio of the coupled inductors. However, it's important to note that the leakage current in the coupled inductors can result in a voltage spike at the output, which is a drawback of these configurations. Active-switched topologies offer an effective means of increasing the boost-factor using fewer components compared to other extended boost ZSIs. During the ST states, the active switch is turned on, and during the non-shoot-through (non-ST) states, the active switch is turned off. One downside of the active-switched topologies is that the additional switch requires a separate gate driver [18-31].

The classic active ZSI topologies [18-20], due to the low boost-factor ability, bring some drawbacks, and utilizing them, the voltage stress across the power devices is increased. The active switched-inductor boost QZSI [21] has a high voltage boosting ability but, in this structure, the impedance network has a high number of elements. Novel high boost active switched inductor QZSI [22] was presented to solve the low boost ability of the classic topologies. However, this inverter suffers from a high component count on its impedance side, and also, due to the limited duty cycle ratio, control of this inverter becomes difficult. High step-up continuous current active-switched boost QZSIs [23] have the same problems, too. Dual active-switched-capacitor QZSI [24] is another topology that offers high output voltage. However, the dual extra switches need two separate gate driver circuits. Utilizing two isolated gate drivers may increase the cost of the system. In [25], the active-switched boost QZSI with few components was proposed to reduce the number of elements of the impedance network. But the boost-factor of it is low. The main benefit of it is that fewer components count on the impedance side. The presented inverter in [26] can achieve a high boost-factor by adding an active switch on the impedance side. Also, it provides continuous input current and common ground. The problem of this topology is high voltage across passive and active components. In [27], n number of capacitor-based cells and m number of inductor-based cells are added in the impedance side of the basic active-switched-capacitor/switched-inductor QZSI topology [10] to achieve a higher boost-factor. So, new multi-cell structure for active-switched-capacitor/switched-inductor QZSI topology is presented. The high voltage across passive and active components and high number of elements are the problem of the mentioned inverter. By changing the number of components and their position in QZSI with switched inductors and switched capacitors, the topologies in [28] are presented. [29] is a combination of switched inductors and active switched capacitors, which cause a very high boost-factor, but the voltages across all components are very high, too. In refs. [32] and [33] a new active ZSIs is presented. These topologies use a low number of components along with low voltage stress across them. But, the boost-factor of them is low.

In this paper, a new active ZSI is proposed. The advantages of the proposed inverter are the continuous source's current, appropriate boost-factor, a few numbers of components, Low voltage stress on active switch and diodes, Low voltage stress across capacitors, and low volume and size. First, the comprehensive analyses of the proposed topology in different operating modes according to the PWM control method are presented. Then, the comparative analysis of the proposed topology and some conventional topologies from different points of view, such as the boost-factor, total voltages across capacitors, and total blocked voltages across impedance side diodes and active switches are done, and the volume comparison of capacitor and inductors of proposed topology and some conventional topologies are prepared. In the following section, the passive and active components are designed. At the end, the simulation results of the proposed inverter are presented.

2. The Proposed Active Impedance Source Inverter

The power circuit of the proposed impedance-

source inverter is shown in Fig. 1. According to this figure, the proposed topology consists of one active switch (S), four inverter side switches (S_1, S_2, S_3, and S_4), two inductors (L_1, L_2), two capacitors (C_1,C_2), two diodes (D_1,D_2) and one DC input voltage. The power circuit of the proposed inverter is shown for a single-phase state. It is sufficient for three-phase applications to replace the single-phase inverter side switches with a three-phase one. In the following section, the proposed topology is analyzed in detail, and all voltages and current equations are calculated. An appropriate control method is needed to produce three voltage levels at the output. So, a suitable control method is produced. According to the control method, inverter side switches have three operating modes. All switches are on in the first operating mode; in the second operating mode, S1 and S4 are on; and in the third operating mode, S_2 and S_3 are on. The first operating mode is the ST state, and the second and third operating modes are the non-ST state. According to the structure of the proposed topology, the diodes are turned off due to the reverse bias when switch S is turned on. Consequently, the input voltage source is protected from a short circuit. According to the given description of the control method, the presented control method in Fig. 2 can be used.

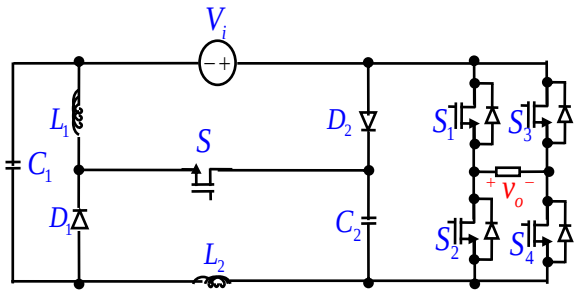


Fig. 1. Schematic of the proposed impedance-source inverters

2-1. Presented Control Method

Fig. 2 shows the logical diagram of the used control method. According to this figure, the logical diagram has three gate signals for all switches (S_1,S_4), (S_2,S_3), and (S_a,S_b). To create these signals, first, two constant reference signals (U_{ST1} and U_{ST2}) are compared with a triangular carrier signal (U_{tri}) to produce H_1 and H_2. Then by comparing the U'_{step} with H_1 and U_{step} with H_2 and by using AND gate, the signals ST_1 and ST_2 are produced. In the end, by using the OR gate and comparing the U_{step} with ST_1 and U'_{step} with ST_2, the gate signal of switches (G_{S1}, … , G_{S4} and G_{Sa},G_{Sb}) will be created. The absolute mathematical value of subtraction of the gate signals of switches S_1 and S_2 is required to generate the gate signals of switches S_a and S_b.

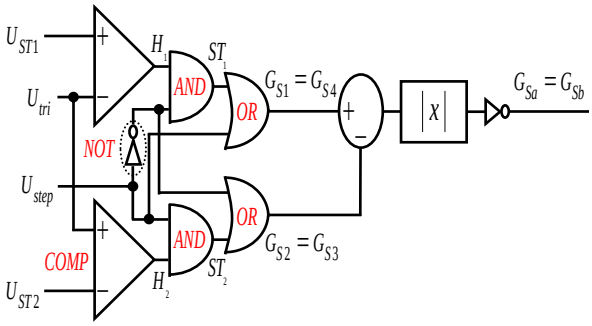


Fig. 2. Logical diagram of presented control method

Fig. 3 shows the waveforms of the presented control method. According to this figure, each period has four operating modes, including two ST and two non-ST states.

It is essential to mention that U_{step} is the square waveform with a positive pulse width in the first half period, and U'_{step} is the square waveform with a negative pulse width in the second half period. Furthermore, the value of the carrier signal frequency is much more than the value of the reference signal. ($f_{car} >> f_{ref}$).

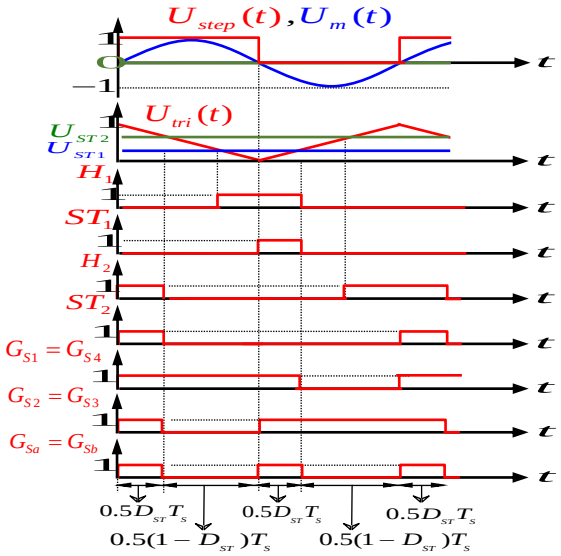


Fig. 3. The waveforms of the presented control method

2-2. Operating Modes of the Proposed Topology

Fig. 3 shows the proposed topology's equivalent circuit. The proposed topology in different operating modes is analyzed in detail, and the voltage and current equations in every operating mode are extracted.

2-2-1. First Operating Mode ($0 < t < 0.5\,D_{ST}T_s$)

In the first operating mode, all switches (S_1, S_2, S_3, and S_4) are turned on, and all diodes (D_1 and D_2) are turned off, as shown in Fig. 4a. The voltage across the diodes confirms this condition. By using Kirchhoff's Voltage Law (KVL), the voltages of the diodes and the voltage across the inductors in the ST state can be calculated:

$$\begin{cases} v_{D1} = -v_{L2} - v_{C2} \\ v_{D2} = -v_{C2} \end{cases} \quad (1)$$

$$\begin{cases} v_{L1} = V_i + V_{C2} \\ v_{L2} = V_i + V_{C1} \end{cases} \quad (2)$$

During this operating mode, the current flowing through the capacitors can be determined as follows:

$$\begin{cases} i_{C1} = -I_{L2} \\ i_{C2} = -I_{L1} \end{cases} \quad (3)$$

These equations demonstrate that the voltages across the inductors increase in the ST state.
Next, the current of the DC link can be obtained:

$$i_{dc} = I_{L1} - i_{C1} \quad (4)$$

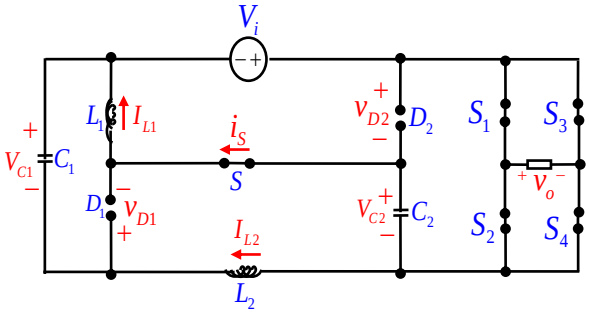
In this operating mode, the output voltage is zero because the switches of the H-bridge cell are on.

2-2-2. Second Operating Mode ($0.5D_{ST}T_s < t < 0.5T_s$)

In Fig. 4b, the non-ST state of the proposed topology is shown. In this figure, switches S_1 and S_4 are turned on to generate a positive output voltage. As a result, switches S_2, S_3, and S are turned off, and diodes D_1 and D_2 are in direct bias. In this operating mode, the current through capacitors increases while the voltages across inductors decrease. This leads to the output voltage reaching its maximum. All equations can be calculated as follows:

$$\begin{cases} i_{C1} = I_{L1} - I_{L2} \\ i_{C2} = I_{L2} - i_o \end{cases} \quad (5)$$

$$\begin{cases} v_{L1} = -V_{C1} \\ v_{L2} = V_i + V_{C1} - V_{C2} \\ v_{dc,\max} = V_{o,\max} = V_{C2} \end{cases} \quad (6)$$



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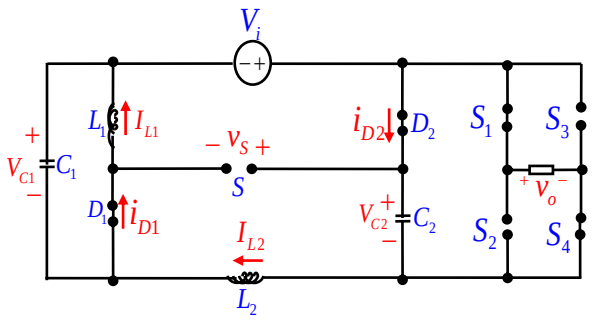

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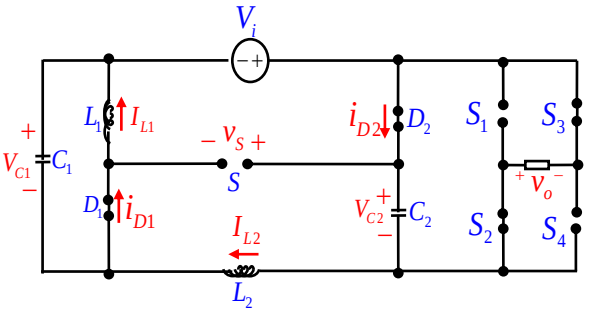


(c)

Fig. 4. Equivalent circuits, (a) First and third operating modes, (b) Second operating mode, (c) Fourth operating mode

2-2-3. Third Operating Mode ($0.5T_s < t < 0.5(1 + D_{ST})T_s$)

As seen in Fig. 4, the equivalent circuits of the first and third operating modes are the same. So, all the first operating mode equations are valid for the third operating mode.

2-2-4. Fourth Operating Mode ($0.5(1 + D_{ST})T_s < t < T_s$)

According to Fig. 4c, switches S_2 and S_3 are turned on to produce a negative output voltage. So, the switches S_1, S_4, and S are turned off, and diodes D_1 and D_2 are in direct bias. Due to the similarity of the equivalent circuits of the second and fourth operating modes, the Equations (8)-(11) are the same, and the output voltage is at its minimum.
For output voltage, we have:

$$v_o = v_{o,\min} = -v_{dc,\max} \quad (7)$$

2-3. Calculation of Boost-Factor

A principle named the volts-second law is used to obtain the boost-factor. Subsequently, the following equation can be written:

$$\int_0^{T_S} v_L dt = 0 \quad (8)$$

By using (2) and (6) the above equation is changed to:

$$(V_{C2}+V_i)D_{ST}+(-V_{C1})(1-D_{ST})=0 \quad (9)$$

$$(V_i+V_{C1})D_{ST}+(V_i+V_{C1}-V_{C2})(1-D_{ST})=0 \quad (10)$$

From the above equations, the average voltages across capacitors can be calculated as follows:

$$V_{C1}=\frac{D_{ST}(2-D_{ST})}{{D_{ST}}^2-3D_{ST}+1}V_i \quad (11)$$

$$V_{C2}=\frac{V_i}{{D_{ST}}^2-3D_{ST}+1} \quad (12)$$

By using (6) and (12), the output maximum DC voltage can be obtained:

$$v_{dc.\max}=\frac{1}{{D_{ST}}^2-3D_{ST}+1}V_i=BV_i \quad (13)$$

In the above equation, B is a boost-factor. So, we can write:

$$v_{o,\max}=-v_{o,\min}=\frac{V_i}{{D_{ST}}^2-3D_{ST}+1} \quad (14)$$

2-4. Design Considerations

This section is intended for the design of passive (inductors and capacitors) and active (switches and diodes) elements. The ripple value of the inductors' current is necessary to get the values of the inductors. To obtain this ripple value, the formula of $v_L=L\frac{di_L}{dt}$ is used. At first, we need to have the voltage of the inductors in one operating mode. For this reason, the first operating mode is used. Then, according to this equation, by using (2), we have:

$$V_{C2}+V_i=2L_1\frac{\Delta i_{L1}}{D_{ST}T_S} \quad (15)$$

$$V_{C1}+V_i=2L_2\frac{\Delta i_{L2}}{D_{ST}T_S} \quad (16)$$

By having (11) and (12), the current ripple value of L_1 and L_2 are calculated as:

$$\Delta i_{L1}=\left|\frac{({D_{ST}}^2-3D_{ST}+2)D_{ST}}{2L_1f_S({D_{ST}}^2-3D_{ST}+1)}V_i\right| \quad (17)$$

$$\Delta i_{L2}=\left|\frac{(1-D_{ST})D_{ST}}{2L_2f_S({D_{ST}}^2-3D_{ST}+1)}V_i\right| \quad (18)$$

The above equations show that by increasing the switching frequency and inductance of inductors, the ripple values are decreased.

In continuation, the voltage ripple of capacitors must be calculated. For this reason, the equation $i_C=C\frac{dv_C}{dt}$ is used. The first operating mode calculates the capacitor voltage ripple as in the previous case. By using (3), we can write:

$$\Delta v_{C1}=\frac{D_{ST}T_SI_{L2}}{2C_1} \quad (19)$$

$$\Delta v_{C2}=\frac{D_{ST}T_SI_{L1}}{2C_2} \quad (20)$$

As is clear from the above equations, the average inductor's current is fundamental to determining capacitors voltage ripple. So, in the following, the average inductor's current is calculated. A principle named ampere-second law is applied to calculate this value. According to this law, the average current value through a capacitor in one period equals zero. In other words:

$$\int_0^{T_s} i_{C1}=\int_0^{T_s} i_{C2}=0 \quad (21)$$

By using (3) and (5), the above equation can be rewritten again as follows:

$$-I_{L2}D_{ST}T_S+(1-D_{ST})(I_{L1}-I_{L2})T_S=0 \quad (22)$$

$$-I_{L1}D_{ST}T_S+(1-D_{ST})(I_{L2}-i_O)T_S=0 \quad (23)$$

By simplifying and substituting (14) in the above equation, the values of the inductors' current are calculated as follows:

$$I_{L1}=\frac{(1-D_{ST})V_{i4}}{R({D_{ST}}^2-3D_{ST}+1)^2} \quad (24)$$

$$I_{L2}=\frac{(1-D_{ST})^2V_{i4}}{R({D_{ST}}^2-3D_{ST}+1)^2} \quad (25)$$

So, the capacitors' voltage ripple is obtained:

$$\Delta V_{C1}=\left|\frac{D_{ST}(1-D_{ST})^2V_{i4}}{2RC_1f_S({D_{ST}}^2-3D_{ST}+1)^2}\right| \quad (26)$$

$$\Delta V_{C2}=\left|\frac{D_{ST}(1-D_{ST})V_{i4}}{2RC_2f_S({D_{ST}}^2-3D_{ST}+1)^2}\right| \quad (27)$$

In the above equations, R is an ohmic value of output resistance.

To achieve the proper capacitance for capacitors and inductance for inductors, we need to know the acceptable values for inductor current ripple and capacitor voltage ripple as a percentage ($|\Delta i_L|=x_L\%\ I_L$ and $|\Delta v_C|=x_C\%\ V_C$). Using the equations given and substituting the acceptable values for the inductor current and capacitor voltage ripple, we can determine the suitable capacitance for capacitors and inductance for inductors.

$$L_1=\frac{D_{ST}({D_{ST}}^2-3D_{ST}+2)({D_{ST}}^2-3D_{ST}+1)R}{2f_S(1-D_{ST})x_{L1}\%} \quad (28)$$

$$L_2=\frac{D_{ST}({D_{ST}}^2-3D_{ST}+1)R}{2f_S(1-D_{ST})x_{L2}\%} \quad (29)$$

$$C_1=\frac{(1-D_{ST})^2}{2Rf_S({D_{ST}}^2-3D_{ST}+1)(D_{ST}-2)x_{C1}\%} \quad (30)$$

$$C_2=\frac{D_{ST}(1-D_{ST})}{2Rf_S({D_{ST}}^2-3D_{ST}+1)x_{C2}\%} \quad (31)$$

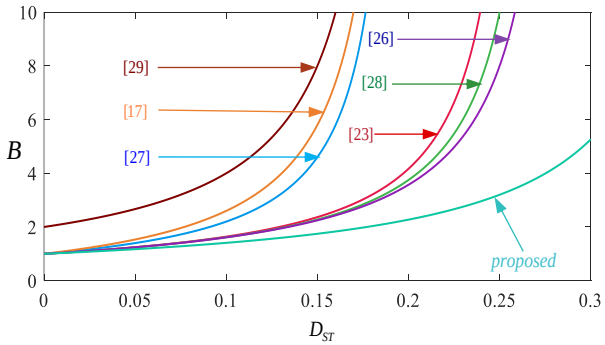
In the following, all operating modes of the proposed topology are analyzed, and the maximum voltage and current of semiconductors of the proposed topology are achieved. Subsequently, in Table 1, the nominal values of those semiconductors are shown.

Table 1. The maximum voltages and currents of semiconductors of the proposed topology

Active components	voltage	current
PIV_{D_1}	$\frac{2-D_{ST}}{{D_{ST}}^2-3D_{ST}+1}V_i$	$\frac{(1-D_{ST})V_i}{R({D_{ST}}^2-3D_{ST}+1)^2}$
PIV_{D_2}	$\frac{1}{{D_{ST}}^2-3D_{ST}+1}V_i$	$\frac{D_{ST}V_i}{R({D_{ST}}^2-3D_{ST}+1)^2}$
V_S	$\frac{1-D_{ST}}{{D_{ST}}^2-3D_{ST}+1}V_i$	$\frac{(1-D_{ST})V_i}{R({D_{ST}}^2-3D_{ST}+1)^2}$
$V_{S_1}=\ldots=V_{S_4}$	$\frac{1}{{D_{ST}}^2-3D_{ST}+1}V_i$	$\frac{V_i}{({D_{ST}}^2-3D_{ST}+1)R}$

3. Comparative Study

The boost-factor, total voltages across capacitors, total blocked voltages across impedance side diodes, and active switches' comparisons are shown in Fig. 5. The comparative analysis with components counts is also shown in Fig. 6. According to Fig. 5b, the proposed topology has a lower total voltage blocked across capacitors than conventional ZSIs. By analyzing Fig. 6, it can be seen that the proposed topology and [23,26,27] have the same number of capacitors in their structures, and [17] have a lower number of capacitors. Still, the proposed topology can achieve a lower total voltage blocked across capacitors, which causes lower volume and size. Actually, according to Figs. 5c and 5d, the proposed topology has lower voltage blocked on diodes and active switches, too. Regarding the boost-factor and Fig. 5a, the boost-factor of the proposed topology is lower than other conventional topologies. Still, it can be seen that the high sensitivity of changing D_{st} is seen in other conventional topologies. So, the proposed topology has an appropriate boost-factor with a low number of elements and lower voltage stress on active and passive components without any sensitivity for D_{st}, which reduces the volume and cost and increases the reliability of the proposed topology.



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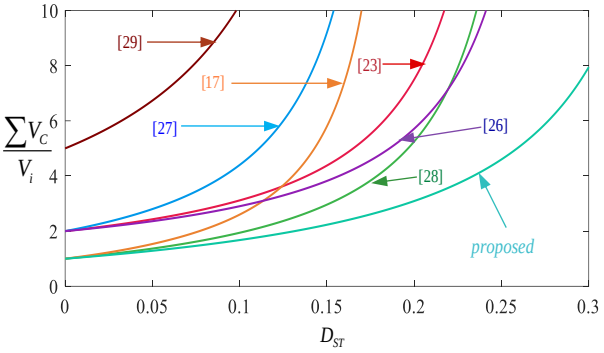

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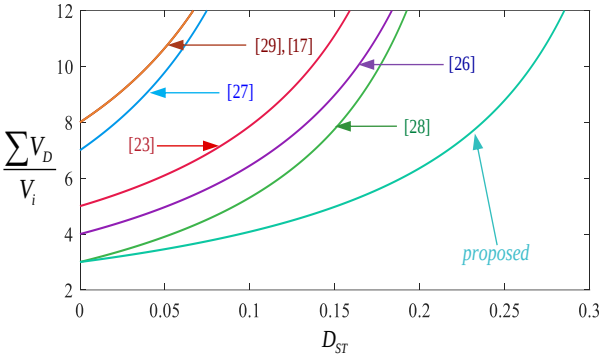

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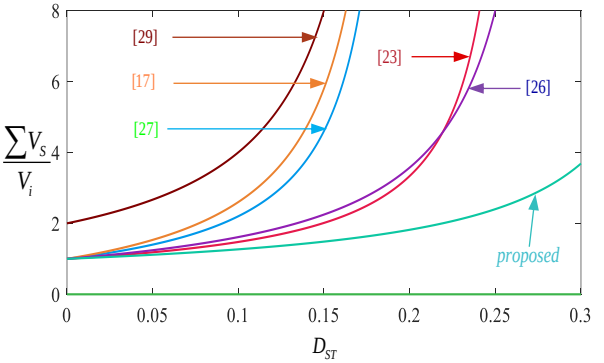


(d)

Fig. 5. The comparative diagrams between all topologies of proposed topologies, (a) Boost-factor, (b) Total voltages across capacitors, (c) Total blocked voltages across diodes, (d) Total blocked voltages across impedance side switches

Table 2. The comparison parameter of the proposed topology and conventional topologies

	B	$\sum \frac{V_C}{V_i}$	$\sum \frac{V_D}{V_i}$	$\sum \frac{V_S}{V_i}$
Proposed	$\frac{1}{{D_{ST}}^2 - 3D_{ST} + 1}$	$-2{D_{ST}}^2 + 2D_{ST} + 1$	$(3 - D_{ST})B$	$(1 - D_{ST})B$
[17]	$\frac{1 + 3D_{ST}}{1 - 5D_{ST}}$	B	$8B$	$(1 - 3D_{ST})B$
[23]	$\frac{1}{{D_{ST}}^2 - 4D_{ST} + 1}$	$(2 - D_{ST})B$	$(5 - 2D_{ST})B$	$(1 - D_{ST})B$
[26]	$\frac{1}{2{D_{ST}}^2 - 4D_{ST} + 1}$	$(2 - 2D_{ST})B$	$4B$	B
[27]	$\frac{1 + D_{ST}}{1 - 5D_{ST}}$	$(2 + 2D_{ST})B$	$(7 + 7D_{ST})B$	$(1 + D_{ST})B$
[28]	$\frac{1 + D_{ST}}{-2{D_{ST}}^2 - 3D_{ST} + 1}$	$(1 + D_{ST}) * (1 + 2D_{ST})B$	${D_{ST}}^2 + 6D_{ST} + 3$	0
[29]	$\frac{2}{1 - 5D_{ST}}$	$(5 + D_{ST})B$	$8B$	$2B$

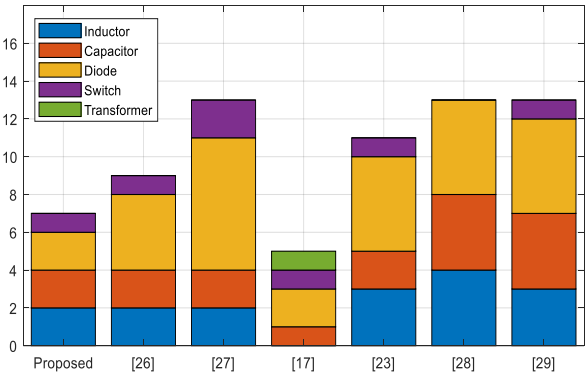


Fig. 6. Bar chart of the number of elements

First, the power density of the proposed topology and some conventional topologies are extracted to evaluate the quality of the proposed topology in terms of volume and weight. The power density of the proposed topology and conventional topologies is influenced by calculating the volumes of its inductors and capacitors. The inductor volume, associated with stored energy (W_L=1/2LI^2), is divided by the inductor's volumetric energy density ($\rho_{E,L}$). The total inductors volume ($V_{inductors}$) for the proposed topology is shown in (32).

On the other hand, the capacitor volume is calculated by dividing its stored energy (W_C=1/2CV^2) by the volumetric energy density $\rho_{E,C}$. The total capacitor volume ($V_{capacitor}$) for the proposed topology is obtained as (33).

Finally, the overall volume metric of the proposed topology ($V_{converter}$) is the sum of relationships (32) and (33), which can be written as (34).

$$V_{inductors} = \frac{\sum E_{Li}}{\rho_{E,L}} = \frac{(-2{D_{ST}}^7 + {D_{ST}}^6 + 23{D_{ST}}^5 - 51{D_{ST}}^4 + 40{D_{ST}}^3 - 14{D_{ST}}^2 + 3D_{ST})P_o}{4({D_{ST}}^2 - 3D + 1)^2 x\% f_s \rho_{E,L}} \tag{32}$$

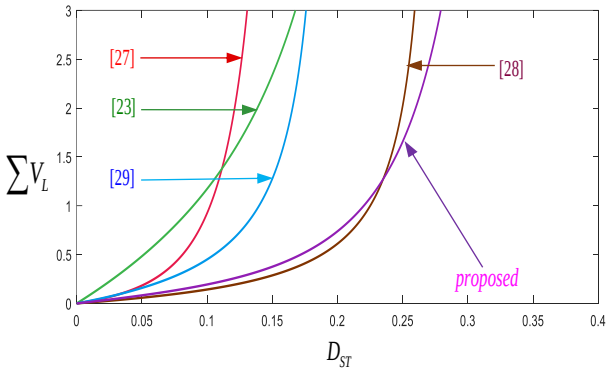
$$V_{capacitor} = \frac{\sum E_{Ci}}{\rho_{E,C}} = \frac{0.5D_{ST}(D_{ST} - 1)^3 P_o}{({D_{ST}}^2 - 3D + 1) y\% f_s \rho_{E,C}} \tag{33}$$

$$V_{converter} = \left(\frac{(-2{D_{ST}}^7 + {D_{ST}}^6 + 23{D_{ST}}^5 - 51{D_{ST}}^4 + 40{D_{ST}}^3 - 14{D_{ST}}^2 + 3D_{ST})}{4({D_{ST}}^2 - 3D + 1)^2 x\% \rho_{E,L}} + \frac{0.5D_{ST}(D_{ST} - 1)^3}{({D_{ST}}^2 - 3D_{ST} + 1) y\% \rho_{E,C}}\right)\frac{P_o}{f_s} \tag{34}$$

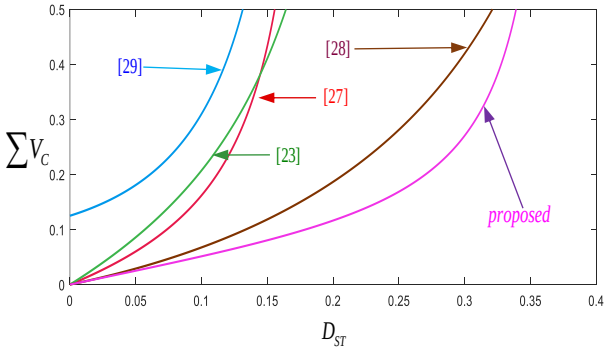
The equations for the volume comparison of the proposed topology and some conventional topologies are shown in Table 3. Based on theoretically calculated relationships from Table 3, a comparative diagram of the volumetric of all inductors and capacitors versus the duty cycle is presented in Fig. 9. Based on Fig. 7a and 7b, it can be concluded that the proposed topology shows significant improvements in terms of volume and power density when compared to the counterparts.

Table 3. The volume comparison of the proposed topology and some conventional topologies

References	Passive components volume,/$T_S P_o$
Proposed	$\frac{(-2D_{ST}^{7}+D_{ST}^{6}+23D_{ST}^{5}-51D_{ST}^{4}+40D_{ST}^{3}-14D_{ST}^{2}+3D_{ST})}{4(D_{ST}^{2}-3D+1)^{2}x\%\rho_{E,L}}+\frac{0.5D_{ST}(D_{ST}-1)^{3}}{(D_{ST}^{2}-3D_{ST}+1)y\%\rho_{E,C}}$
[27]	$\frac{2D_{ST}(1+D_{ST})(1-2D_{ST})(1-D_{ST})^{4}}{(1-5D_{ST})^{3}x\%\rho_{E,L}}+\frac{D_{ST}(1-D_{ST})^{2}}{(1-5D_{ST})y\%_{s}\rho_{E,C}}$
[23]	$\frac{(17D_{ST}^{2}-36D_{ST}+67)(1-D_{ST})D_{ST}}{8(D_{ST}^{2}-4D_{ST}+1)x\%\rho_{E,L}}+\frac{(-0.5D_{ST}^{2}-1.5+D_{ST})(D_{ST}-1)D_{ST}}{(D_{ST}^{2}-4D_{ST}+1)y\%_{s}\rho_{E,C}}$
[28]	$\frac{D_{ST}(1-D_{ST})^{2}(2+D_{ST})}{4(1+4D)(D_{ST}-0.5)(1-3D_{ST}-2D_{ST}^{2})x\%\rho_{E,L}}+\frac{(0.5+D_{ST})(D_{ST}-1)D_{ST}}{(2D_{ST}-1)y\%_{s}\rho_{E,C}}$
[29]	$\frac{5D_{ST}(D_{ST}-1)}{2(5D_{ST}-1)x\%\rho_{E,L}}+\frac{14D_{ST}^{2}+D_{ST}+1}{8(1-5D_{ST})y\%_{s}\rho_{E,C}}$



(a)



(b)

Fig. 7. Total volumetric comparison: (a) inductors; (b) capacitors.

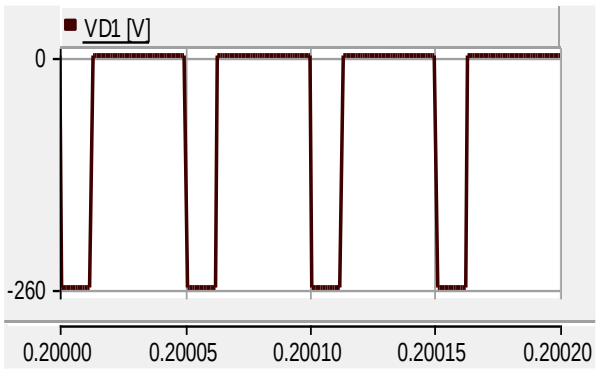
To evaluate the cost of the proposed topology in terms of the number of elements, as shown in Fig. 6, the proposed topology has fewer number of components than many conventional topologies. Also, to determine the cost of each component of the proposed topology, Figs. 5 and 7 show the less nominal value of total voltages across diodes and active switches and less total capacitor voltages and current through inductors than conventional topologies. So, it can be concluded that the total cost of the proposed topology is lower than that of other existing topologies.

4. Simulation Results

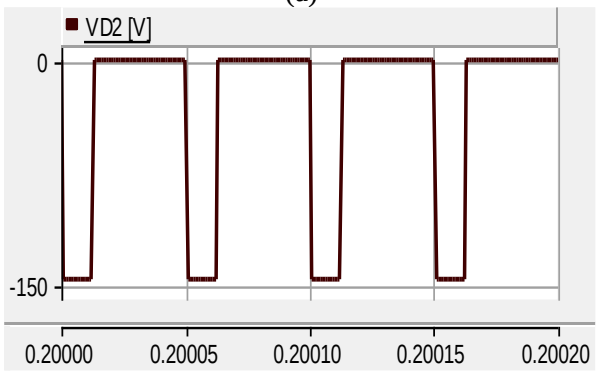
The simulation results are used to reconfirm the theoretical analysis. So, the suitable amounts of inductors and capacitors should be calculated. First, the used control method is similar to Fig. 2 by considering f_{car}=10*kHz*, f_{ref}=50*Hz* and the equation of the modulation index of this control method is $M=1-D_{ST}$. Then, according to (28)-(31) and by considering inductors' current ripple ($x_{L1}\%$ equal to 0.8 and $x_{L2}\%$ equal to 0.7) and capacitors' voltage ripple ($x_{C1}\%$ equal to 0.5 and $x_{C2}\%$ equal to 0.04), switching frequency (f_S equal to 10*kHz*), load output resistance (R_L equal to 50Ω) and D_{ST}=0.24, the amounts of capacitors C_1, C_2 and inductors L_1, L_2 will be 100μF, 68μF,0.8mH and 0.7*mH*, respectively. The input voltage is assumed 50*V*. Figs. 8a and 8b demonstrate the voltage across diodes D_1 and D_2 in simulation results, respectively. These figures not only confirm the condition of ST and non-ST states but also validate the magnitude of the voltages across diodes. In theoretical analysis, based on (1), the voltage values of diodes D_1 and D_2 are equal to 260.66V and 148.10V, respectively, which is consistent with simulation results.

Figs. 8c, d, e, and 8f show the voltage and current through inductors in simulation results, respectively. According to equations of voltage and current of inductors in theoretical analysis, the voltages of the inductor L_1 at the first and second operating modes are equal to 198.10*V* and -62.55*V*, respectively, and the voltages of the inductor L_2 at the first and second operating modes are equal to 112.55*V* and -35.54*V*, respectively. The average value of the current of inductor L_1 is equal to 6.66*A*, and the average value of the current of inductor L_2 is equal to 5.06*A*. By matching these values with Figs. 8c, d, e, and 8f, the validation of the voltage

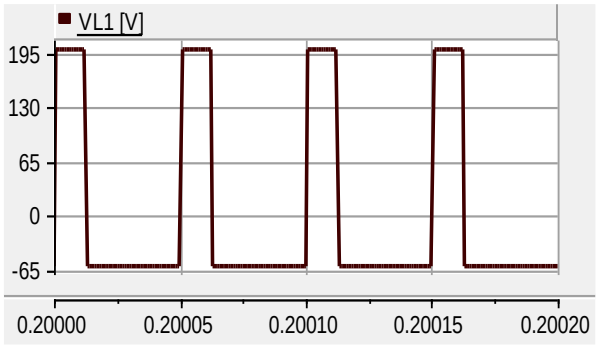
and current of inductors is approved. According to the equations of capacitors' voltage in theoretical analysis, the average voltage value of capacitors C_1 and C_2 equals 62.55V and 148.10V, respectively. Considering Fig. 8g and 8h, the simulation results show that the voltage across capacitors C_1 and C_2 is approximately 62V and 148V, respectively. Comparing the theoretical and simulation results shows a good agreement between them. Figs. 8i and 8j present the input current and output voltage in simulation results, respectively. The input current waveforms in simulation results verify the continuous input current, and the output voltage waveforms in simulation results verify three voltage levels at the output side with a magnitude close to 148V. The trigger pulses of all switches in simulation results are shown in Figs. 8k, l and 8m. These figures approve the correctness of ST and non-ST states of all switches. Fig. 8n is presented to verify the voltage's magnitude across the active switch. It can be seen that the waveform of voltage across active switches verifies the results of the theoretical analysis. The blocked voltage of the impedance side switch (S) is close to 112V. It is essential to mention that the amounts of the blocked voltage of the impedance side switch in the theoretical analysis are equal to 112.55V. So, there is a good agreement between theoretical and simulation results.



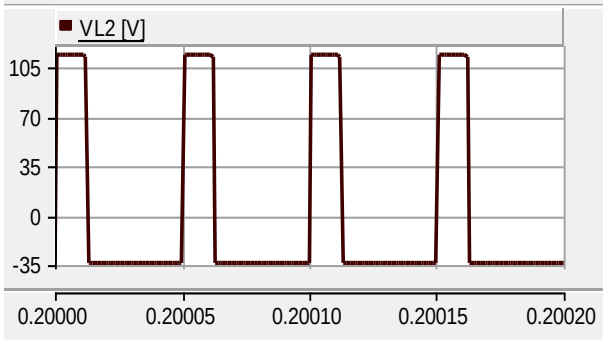
(a)



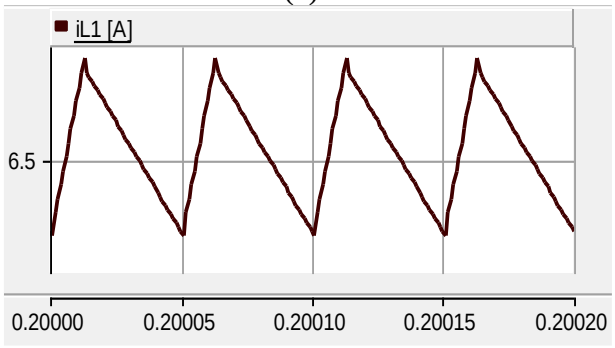
(b)



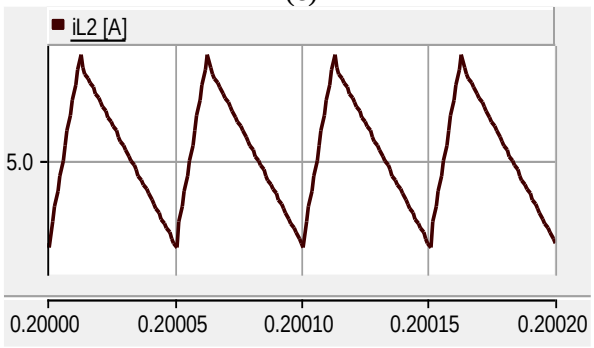
(c)



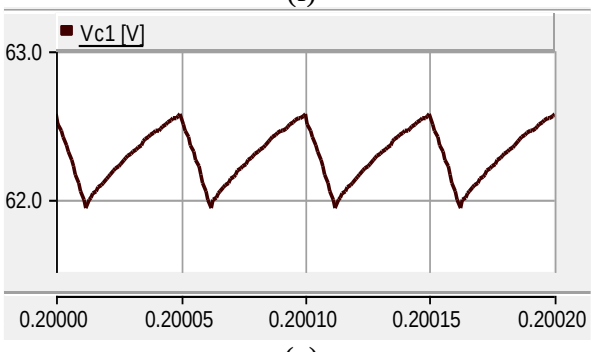
(d)



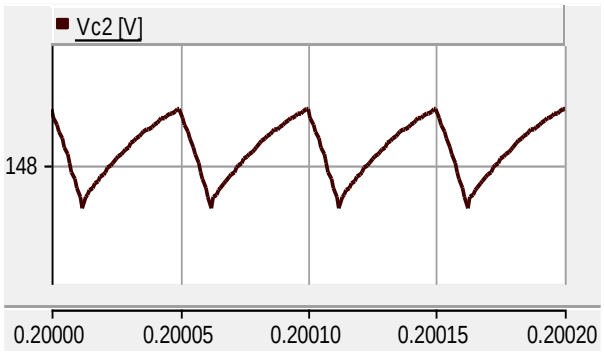
(e)



(f)



(g)



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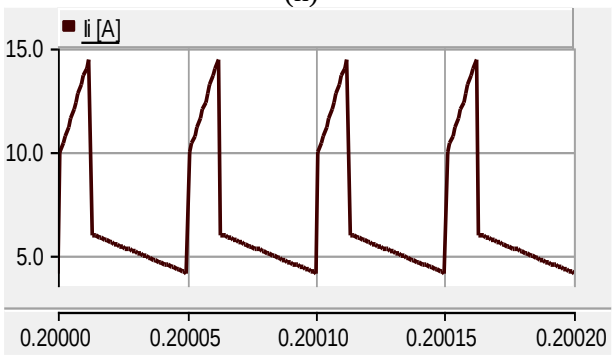
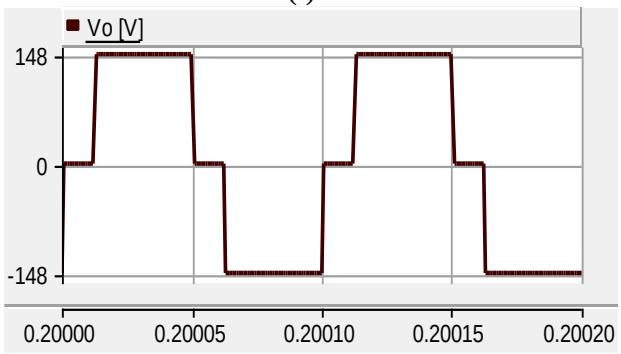


(i)



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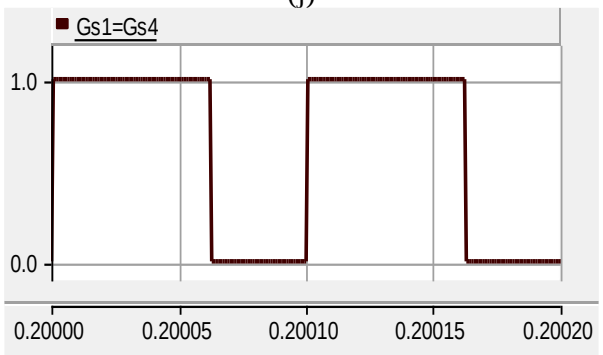
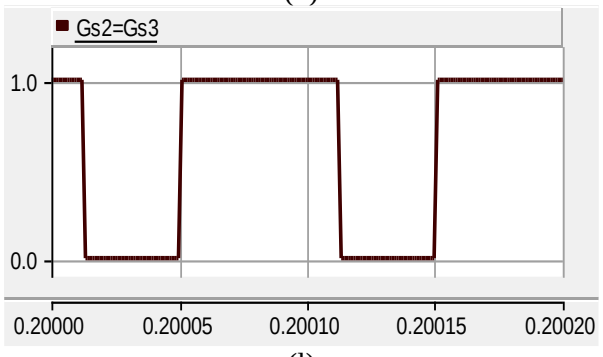
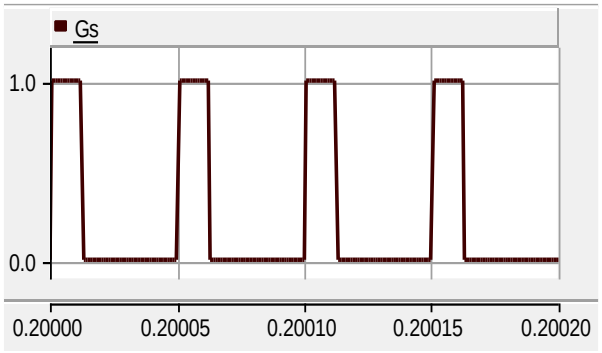


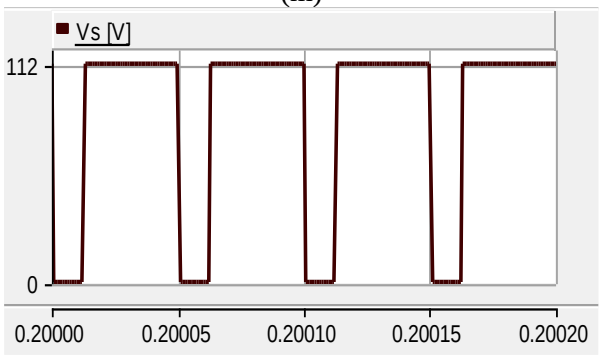
(k)



(l)



(m)



(n)

Fig. 8. Simulation results, (a) Voltage on D_1, (b) Voltage on D_2, (c) Voltage across L_1, (d) Voltages across L_2, (e) Current through L_1, (f) Current through L_2, (g) Coltages across C_1, (h) Voltages across C_2, (i) Input current, (j) Output voltage, (k) The trigger pulses of switches S_1 and S_4, (l) The trigger pulses of switches S_2 and S_3, (m) The trigger pulses of active switch, (n) Voltage on active switch

According to (24), the boost factor of the proposed topology is dependent on the duty cycle. On the other hand, the output voltage can be controlled by adjusting the value of D_{ST}. Also, according to the presented control method, the duty cycle frequency is high. Consequently, this feature of output voltage at a high frequency is suitable for plating technology and meets the requirements of this application.

5. Conclusion

This paper proposed a new active impedance source inverter with lower voltage stress on semiconductor devices compared with some traditional ZSI. First, the proposed topologies' power circuit and the control method were described to create the desired output voltage. Four operating modes of the proposed topology were exhaustively analyzed, and the boost-factor factor was fully calculated. The ideal values of passive and active components were calculated by analyzing all operating modes. Then, a comprehensive analysis was done to check the superiority of the proposed topology versus

conventional inverters from the point of view of the boost factor, the sum of voltages and current stress on capacitors, inductors, diodes, and switches. The power density of the proposed topology and some conventional topologies to evaluate the quality of the proposed topology in terms of volume and weight are extracted. This comparison shows that the proposed topology has a lower power density. finally, to verify the validity of the equations and the correctness of the performance of the proposed topology, the simulation results were added. These simulations' results confirmed the proposed topology's performance and the calculated equations' correctness.

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Biography

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